IN THE CLAIMS

1-4. (Cancelled)

5. (Currently Amended) The method of Claim 13 4, wherein at least one EEPROM device is collocated on the same die as at least one FPGA.

6. (Original) The method of Claim 134, further comprising the step of loading at least one of the programmable logic devices with configuration code from at least one of the EEPROMs.

7-10. (Cancelled)

11. (Currently Amended) A system comprising:

a plurality of interconnected circuit boards, at least two of the plurality of interconnected circuit boards embodying at least one FPGA coupled to a configuration EEPROM of the type capable of being programmed over a serial bus;

wherein at least one EEPROM of a circuit board of the plurality of circuit boards is coupled to a first serial bus, and at least one EEPROM of a circuit board of the plurality of circuit boards is coupled to a second serial bus;

wherein at least one EEPROM of the first serial bus and at least one EEPROM of the second serial bus contains board identification information;

common configuration point apparatus coupled to the first serial bus and to the second serial bus, the common configuration point apparatus further comprising:

selection apparatus for selecting a particular bus of the first and second serial busses; and

coupling apparatus for coupling configuration signals to the particular bus of the plurality of serial busses.

12. (Currently Amended) The system of Claim 11 ~~10~~, wherein the first serial bus and the second serial bus are of the JTAG type.

13. (New) A method of in-system programming of Electrically Erasable Programmable Read Only Memories (EEPROMs), the EEPROMs coupled to provide configuration code to programmable logic devices, each EEPROM being located on a particular circuit board of a plurality of circuit boards of a system and wherein not all EEPROMs are located on the same circuit board, comprising:

providing a plurality of board-specific serial busses of the Joint Test Action Group (JTAG) type, each board-specific serial bus coupling to EEPROMs of a particular circuit board;

coupling the plurality of board-specific serial busses to a common configuration point having selection apparatus;

coupling the common configuration point to configuration apparatus capable of interacting with at least one serial bus to program EEPROMs;

setting the selection apparatus to select a particular board-specific serial bus of the plurality of board-specific serial busses;

reading board identification information through the board-specific serial bus to the configuration apparatus, and verifying compatibility of the configuration code is with a circuit board embodying at least one EEPROM coupled to the board-specific serial bus;

erasing at least one EEPROM coupled to the particular board-specific serial bus;

writing programmable logic device configuration code through the selected board-specific serial bus to the at least one EEPROM; and

wherein the programmable logic device configuration code comprises configuration code for at least one FPGA.

14. (New) The method of Claim 13 further comprising the step of selecting a configuration code from a file containing a plurality of configuration codes according to the board identification information.